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NAVAL POSTGRADUATE SCHOOL

Monterey, California

IMPLEMENTATION OF CONTROL BUS HARDWARE AND UTILIZATION OF THE NAVAL POSTGRADUATE SCHOOL SATELLITE SIGNAL ANALYZER

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Project Report

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The layout, construction, implementation, and testing of a control bus interface board which is compatible with the INTERDATA 7/32 multiplexer bus is presented. The interface board is independently addressable and universal in design. A complete test procedure for isolating faults is included.

ABSTRACT

The layout, construction, implementation, and testing of a control bus interface board which is compatible with the INTERDATA 7/32 multiplexer bus is presented. The interface board is independently addressable and universal in design. A complete test procedure for isolating faults is included.

Volume II of this report describes a special signal processing technique developed in the Naval Postgraduate School Satellite Communications Laboratory. The doppler phenomenon, as it affects neary geostationary satellites, is discussed and suggestions for future research topics are given.

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I. INTRODUCTION

A. BACKGROUND

In March of 1977, the Satellite Communication Laboratory of the Naval Postgraduate School received funding from PME-106-1 of the Naval Electronic Systems Command to develop, design, and construct a Satellite Communications (SATCOM) Signal Analyzer. The purpose of this system is to provide high-speed spectrum analysis and characterization of the outputs of the UHF communication satellite transponders while in orbit and operating. This system is to develop techniques for use in the design of a SATCOM monitoring system for use in Naval Communications Stations. The first reports of this effort include receiver design for the satellite signal analyzer [1] and digital control and processing for a satellite communications monitoring system [2]. Additional refinements have been made and are documented in subsequent reports [3, 4, 5, 6, 7, 8].

This project is part of a series of radio frequency measurement and analysis projects undertaken by this laboratory concerning UHF satellite communications.

B. SPECIFIC GOALS

The specific goals in the development of this system are (1) to develop the necessary equipment to make real-time measurements at the Naval Postgraduate School, and (2) to provide the necessary research and development of real-time

signal analysis techniques and equipment for use in a follow-on version of the Fleet Satellite Monitoring System (FSM) presently in use at Naval Communications Stations to monitor the operation of the GAPFILLER and FLTSAT satellites.

C. SCOPE OF THIS REPORT

Figure 1.1 is a basic block diagram of the Satellite Signal Analyzer. This report describes the heart of the Control Bus Interface which is the Control Bus Interface Printed Circuit Board. The construction, fabrication, and testing of this circuit board and its implementation is documented herein.

D. SATELLITE SIGNAL ANALYZER

The Satellite Signal Analyzer is constructed around an INTERDATA 7/32 minicomputer which provides all the necessary control for most of the equipment in the system. The HEWLETT-PACKARD 9830A Programmable Electronic Calculator acts as the interim controller for all equipment on the IEEE Standard Digital Interface Bus (IEEE-488). Interfacing between the HP-9830A and the INTERDATA 7/32 is via a standard RS-232C Data Communications Link.

Fast Fourier Transforms (FFT's) are provided by the AP-120B Array Processor manufactured by Floating Point Systems. Extremely accurate frequency measurement is provided by phase-locked loop receivers. A HEWLETT-PACKARD 5061A Cesium Beam Frequency Standard provides reference frequencies for all

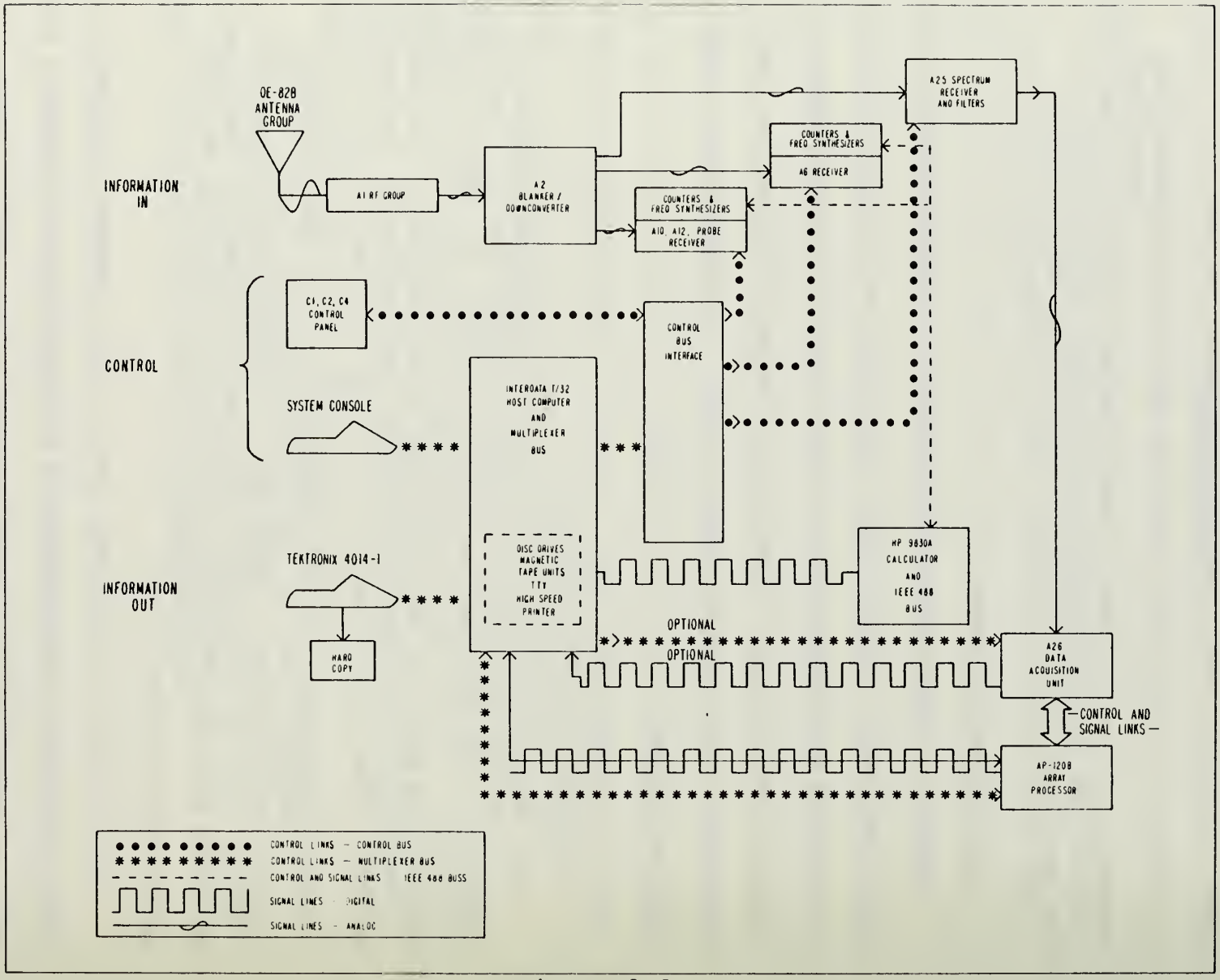


Figure 1.1

Satellite Signal Analyzer

measurements and synthesized equipment.

E. APPROACH

This project was very specific in nature. From a paper design, a working, independently addressable controller had to be fabricated. This controller had to interface with the INTERDATA 7/32 multiplexer bus and yet be flexible enough in design to interface also with any given peripheral device it was desired to control.

Not all programmable laboratory equipment is provided with adapters to allow control or communication via the IEEE-488 bus system. Several of the devices required in the Signal Monitoring and Analyzing projects are not available commercially and need to be built in the laboratory. These include the Control Panel/Switch boards and the various receivers. Both of these classes of equipment require some means of interface to the computer in order to come under program control.

For these reasons, it was decided to build the Control Bus Interface in two parts. The first part, which is the heart of the system, is the Control Bus Interface Board which is universal and independent of the device which it controls. This board is documented in this report in addition to the SCLRO/SATNO Monitor Board, and the Bus Termination boards.

The second part of the Control Bus Interface is the "option" boards which interface a specific peripheral device

to the Control Bus Interface Board. The option board design, construction, and layout is documented in another report [5].

In addition to the hardware development, this report contains test procedures to be used during checkout and troubleshooting.

II. CONTROL BUS INTERFACE

A. HISTORY

Some means to gain access to the INTERDATA 7/32 multiplexer bus had to be developed in order to provide the desired control of peripheral devices. A technique which would allow data to flow to and from the computer with minimum delay was needed. This technique would have to allow for both computer driven I/O and device driven I/O, i.e., the computer must respond to events via the interrupt logic. Data transfers must be independent in the sense that I/O with any device must proceed regardless of the state of any other device.

INTERDATA offers two interface boards that could be used for this purpose, the General Purpose Wire Wrap Board with no presupplied logic but provision for up to 117 Integrated Circuite (IC's), and the Universal Logic Interface with most of the logic required already installed and positions available for 77 more I.C.'s. In either case, if several interfaces are required, 7/32 multiplexer I/O bus loading must be considered and additional chassis and Sub Channel Controller Units would have to be purchased. The cost of these devices, in sufficient quantities, was found to be prohibitively expensive, especially considering the low data rates required for most of the devices.

Several alternatives were considered, including a bus system designed by the National Bureau of Standards called

the NBS Bus. It was finally decided that the most straightforward interface system was one which followed most of the interface standards of INTERDATA but was scaled to simpler needs, and, for the most part, equivalent in a software sense to standard peripheral interfaces.

The Control Bus has been implemented in CAMBION 714 and CAMBION 715 Chassis with wire wrap backplanes. Initially, the hardware developed was implemented by using CAMBION 714 and 715 size wire wrap and copper clad printed circuit boards wired or etched using the facilities of this laboratory and the Electrical Engineering Department. The original structure of this bus is documented [2], however, several minor modifications have been made since.

Basically, the design of the Control Bus Interface Board is very similar to the INTERDATA Universal Logic Interface. Control Bus timing and protocol follows standard INTERDATA I/O convention as specified in [9] with the following exceptions: Data Lines are unidirectional with 8 bits out and 8 bits in. 8 bit addressing is used as 255 total device addresses is considered sufficient. The Control Bus is intended for use with relatively low throughput rate devices with data rates typical of 1 Khz byte rate and below.

B. DESIGN

Reference 2 gives complete Control Bus circuit descriptions and those circuits remain unchanged. Figure 2.1 is the

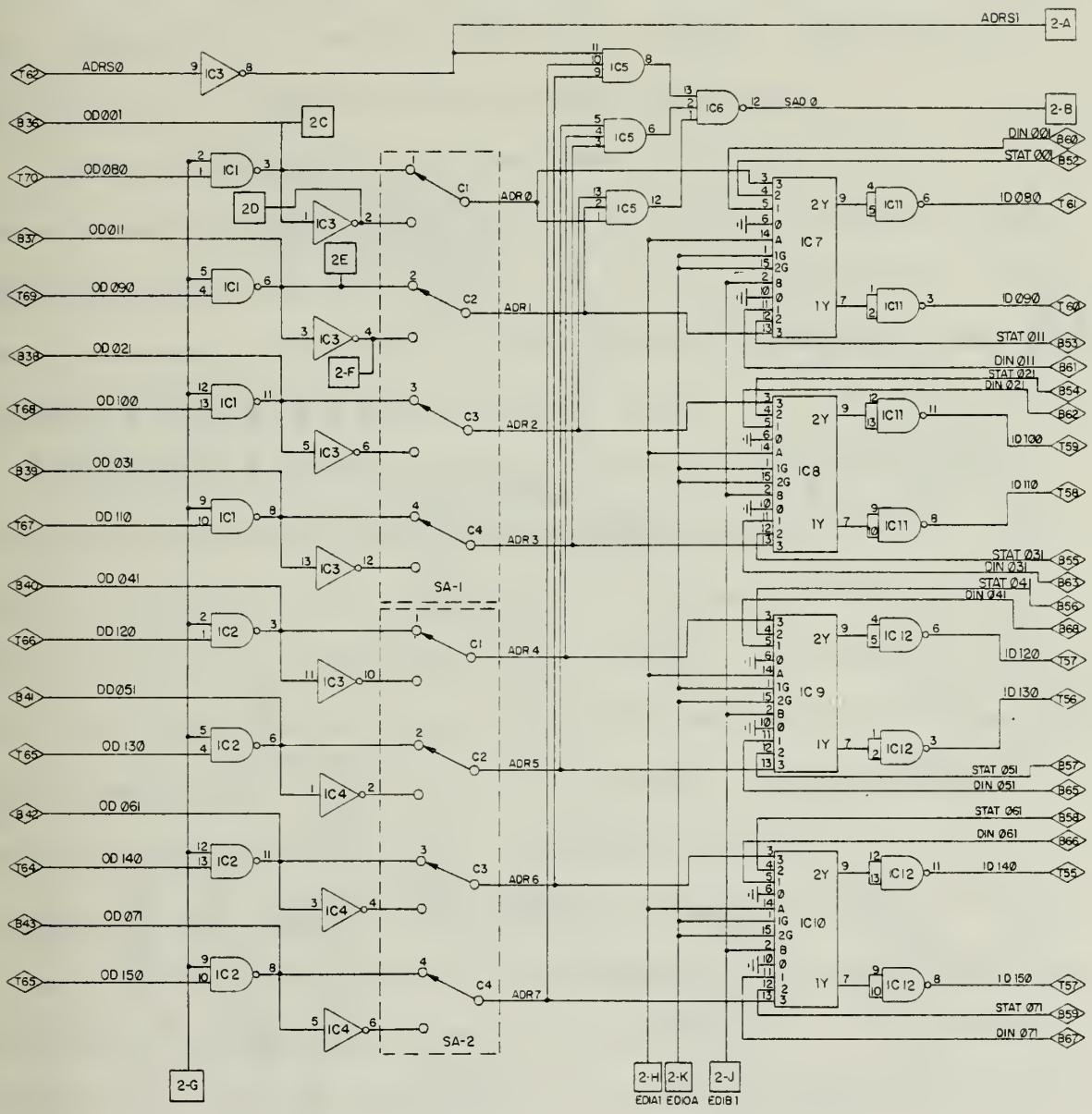


Figure 2.1 (A)

Control Bus Interface Board Schematic

(Part 1)

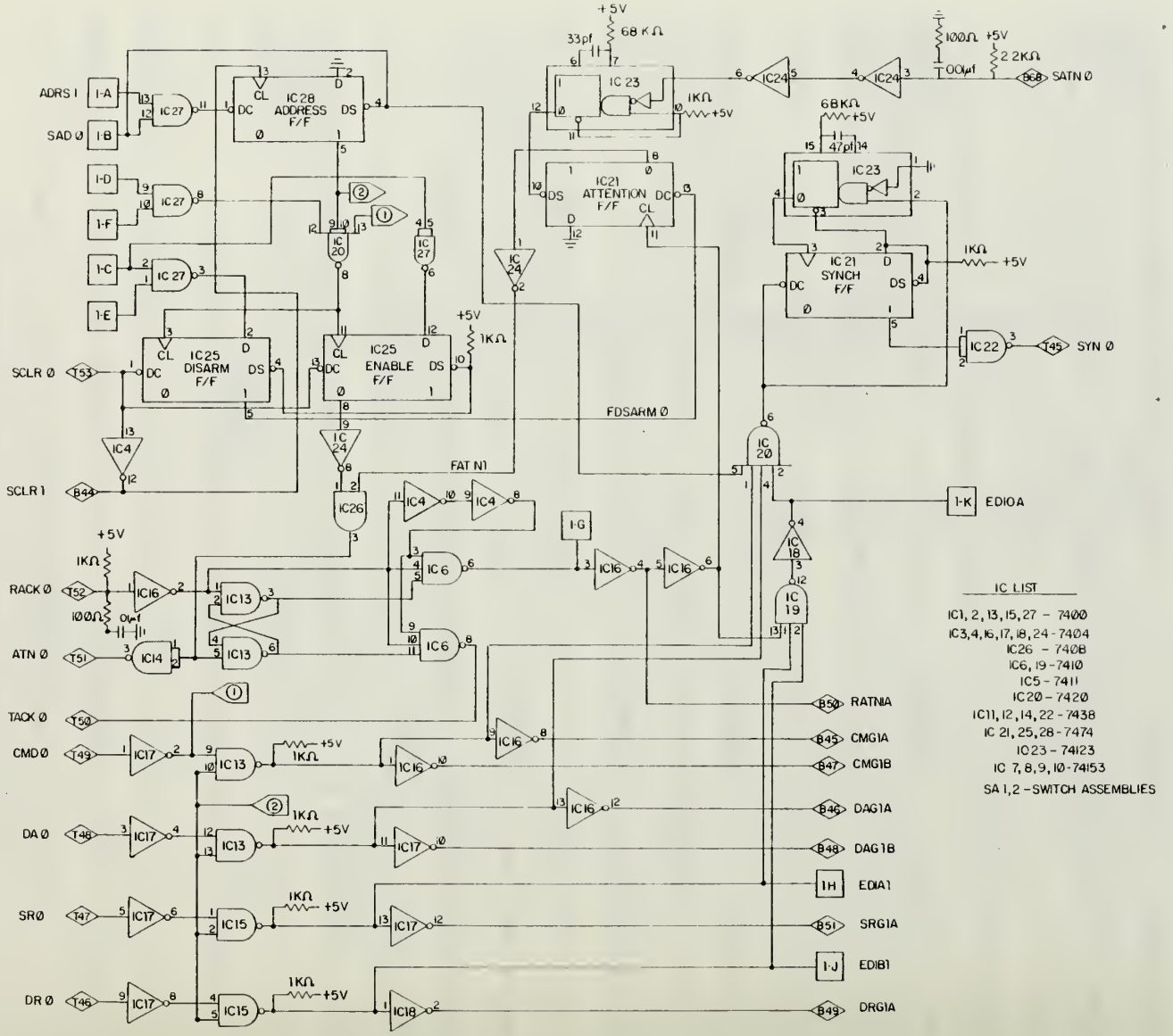


Figure 2.1 (B)

Control Bus Interface Board Schematic

(Part 2)

schematic diagram of the Control Bus Interface Board. From the schematic, it can be seen that a large number of TTL logic IC's are required to realize the design.

The prototype circuit was constructed in a wire wrap version which would allow great flexibility should design changes need to be incorporated. After construction, however, testing proved the circuit design to be sound and the process of printed circuit layout began.

During the testing phase of the prototype Control Bus Interface Board, it was felt that a simple means of statically simulating the INTERDATA 7/32 computer was needed. This would allow testing of the complete Control Bus hardware yet free the computer for other uses during prolonged troubleshooting. As a result, a static Computer Simulator Panel was constructed [5], which can exercise every capability of the entire Control Bus hardware. Used in conjunction with the A29 Interface Test Panel [5], the Computer Simulator has proven to be an invaluable aid in troubleshooting and allows the bus to function independently of any other peripheral devices.

III. PRINTED CIRCUIT LAYOUT

A. METHOD

Given a schematic diagram, constructing a prototype in a wire-wrap version was not difficult. After testing the wire-wrap version, it was felt that printed circuit layout would progress smoothly and a production run of several boards would be done in short order. However, the time spent in design of a layout required a considerable number of man-hours and the only method which seemed to prevail was trial and error.

Paper cut-outs of each IC and the board itself were prepared and after two or three iterations, a rough idea of density and chip placement emerged. This process was extremely time consuming and it was felt that there must be an easier method. Indeed, computer programs exist which aid greatly in PC layout, however, the cost of such software is prohibitive if only a few boards are to be made. There are many companies which can provide these services but they were not economically feasible for the same reason.

The final design was laid out on a nearly transparent plastic grid and cut to twice the size of the desired board. Printed circuit tape was used in the layout as well as tape type transfers for the IC's. Due to the complexity of the circuit and the number of logic elements involved, a double-sided layout was constructed.

The first two or three boards were constructed using pre-cut CAMBION 714 type dual-sided copper clad boards. The use of these boards was considered essential since the edge-connector "fingers" are pre-etched and it was felt that these boards would alleviate connector alignment problems when inserted in the CAMBION Chassis. However, the use of these boards actually caused some problems since the connector fingers are gold-plated and breaks in the foil appeared at the junction of the glod-plated finger and the copper foil. These problems are attributed to the simple etching facilities available to this laboratory. However, when the layout was etched on common dual-sided stock the problem disappeared.

The etching laboratory available does have the capability to silver or gold plate on the copper foil. However, the capability to "plate-through" holes drilled in a board does not exist. This fact required foil pads to be placed wherever a connection had to be made from one side of the board to the other side. But, during construction, an exorbitant amount of time was spent in soldering wire through these foil pads to make a connection. The construction of a single board was taking from six to eight hours each to complete due to the large number of solder connections required. Since thirty-six of these boards were required, it was decided that an alternative was needed.

B. FINAL VERSION

Investigating current methods of printed circuit board fabrication revealed that a run of thirty to fifty baords can be made in industry for a reasonable price. A contract was negotiated with STANFORD APPLIED ENGINEERING of Santa Clara, California, and thirty-six first quality plated-through PC boards were produced for only slightly more cost than the blank boards originally purchased from CAMBION. An important factor in the lower cost was due to having a layout design already completed. These commercially produced boards were ordered with the IC sockets already soldered on the board. This greatly facilitated assembly and construction time dropped from approximately six hours to two hours per board.

The only problems experienced thus far with the commercially produced boards has been a failure of the board to slide easily into the chassis edge connector due to a slight bow in the fiberglass. This is attributed to the fact that the board stock is cut from very large pieces which are very heavy and can develop a bend or set quite easily. A simple fix which works quite well was made by mounting a small length of aluminum U-channel stock across the connector end of the board. This straightens the board and it slides into the connector easily without the danger of bending a pin in the chassis connectors.

Figures 3.1, 3.2 and 3.3 show the final layout and board size. The final design uses a bus structure for power and

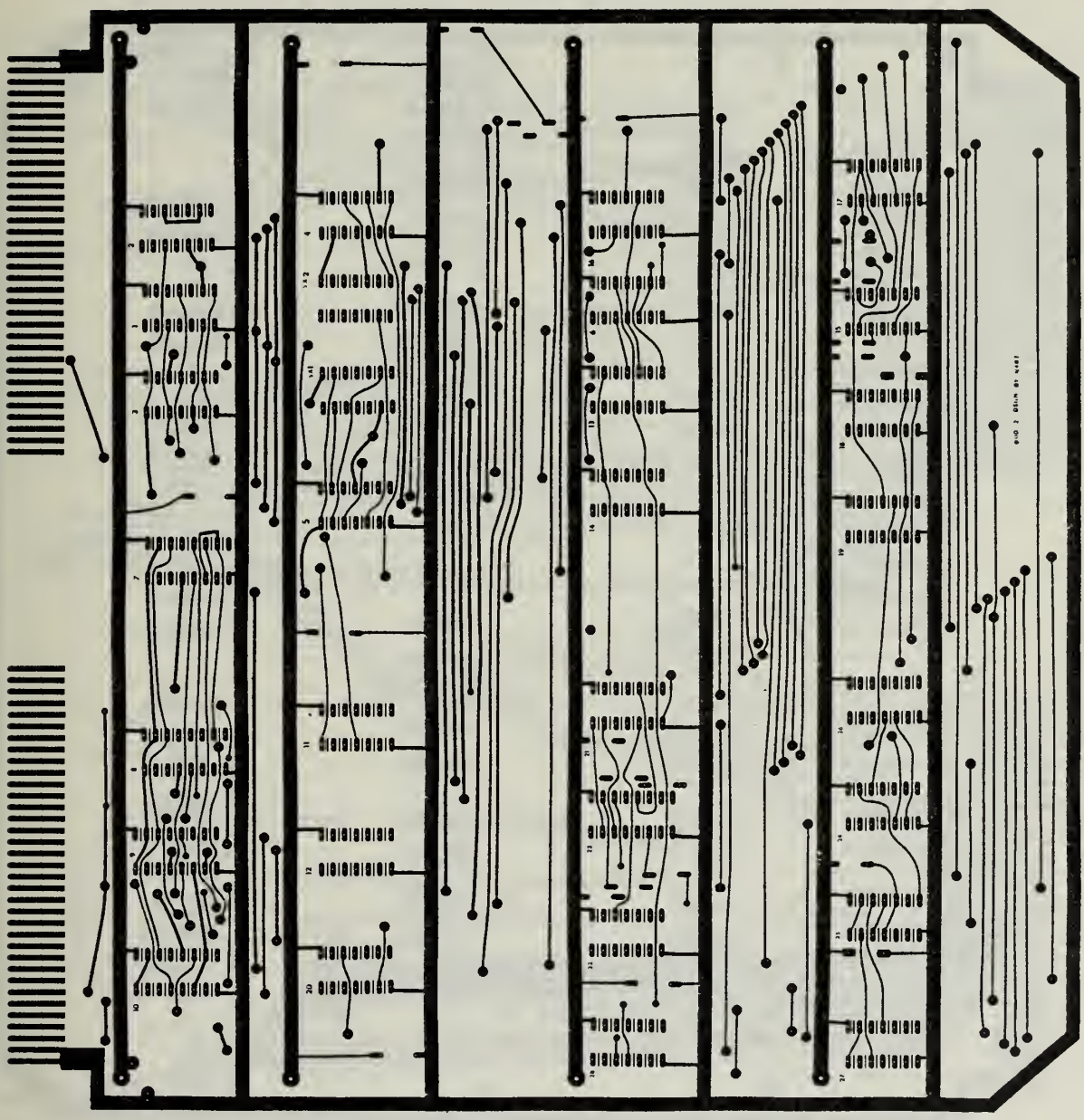


Figure 3.1

Control Bus Interface Printed Circuit Board
(Top or Component Side)

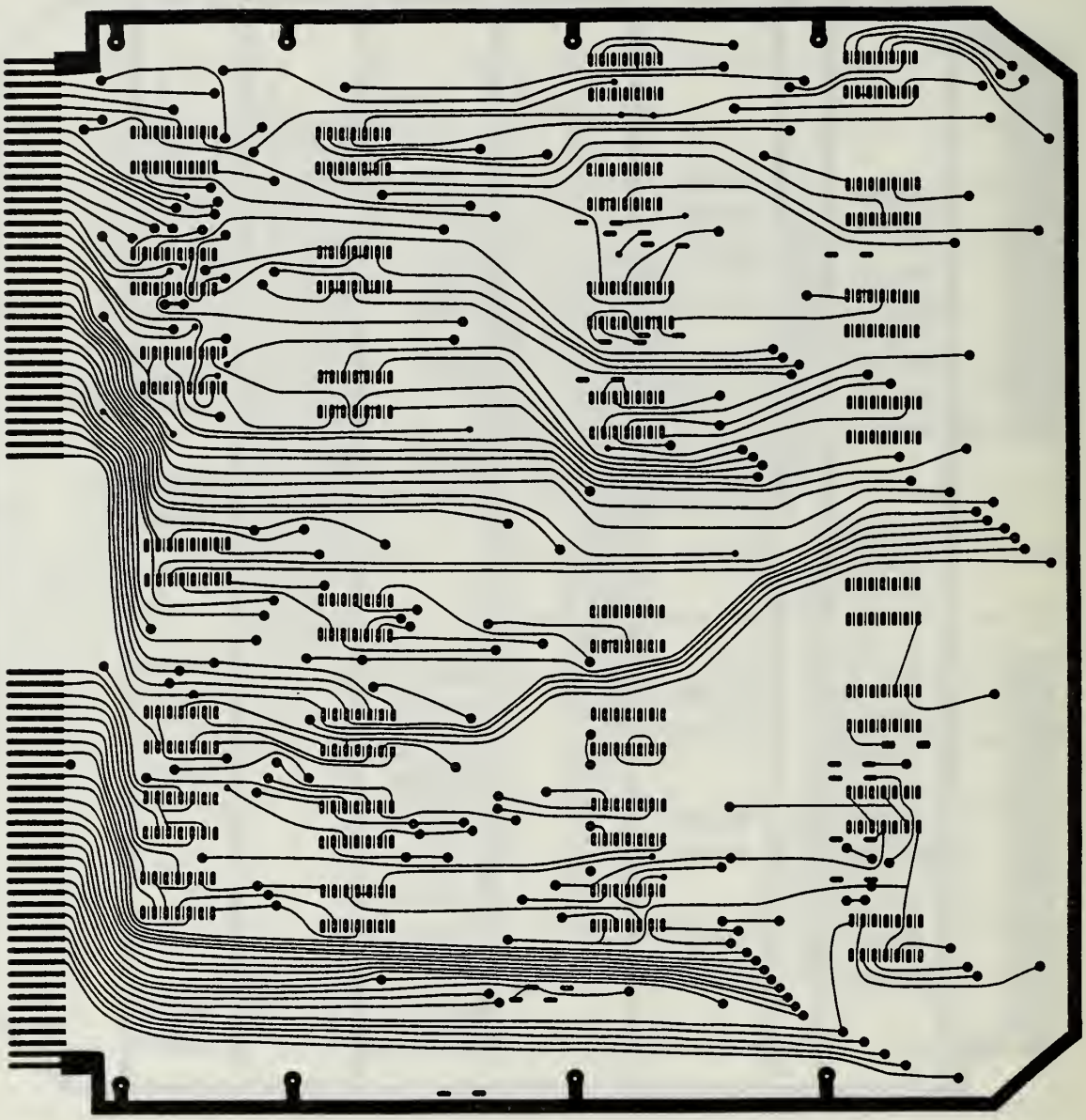


Figure 3.2

Control Bus Interface Printed Circuit Board
(Bottom Side)

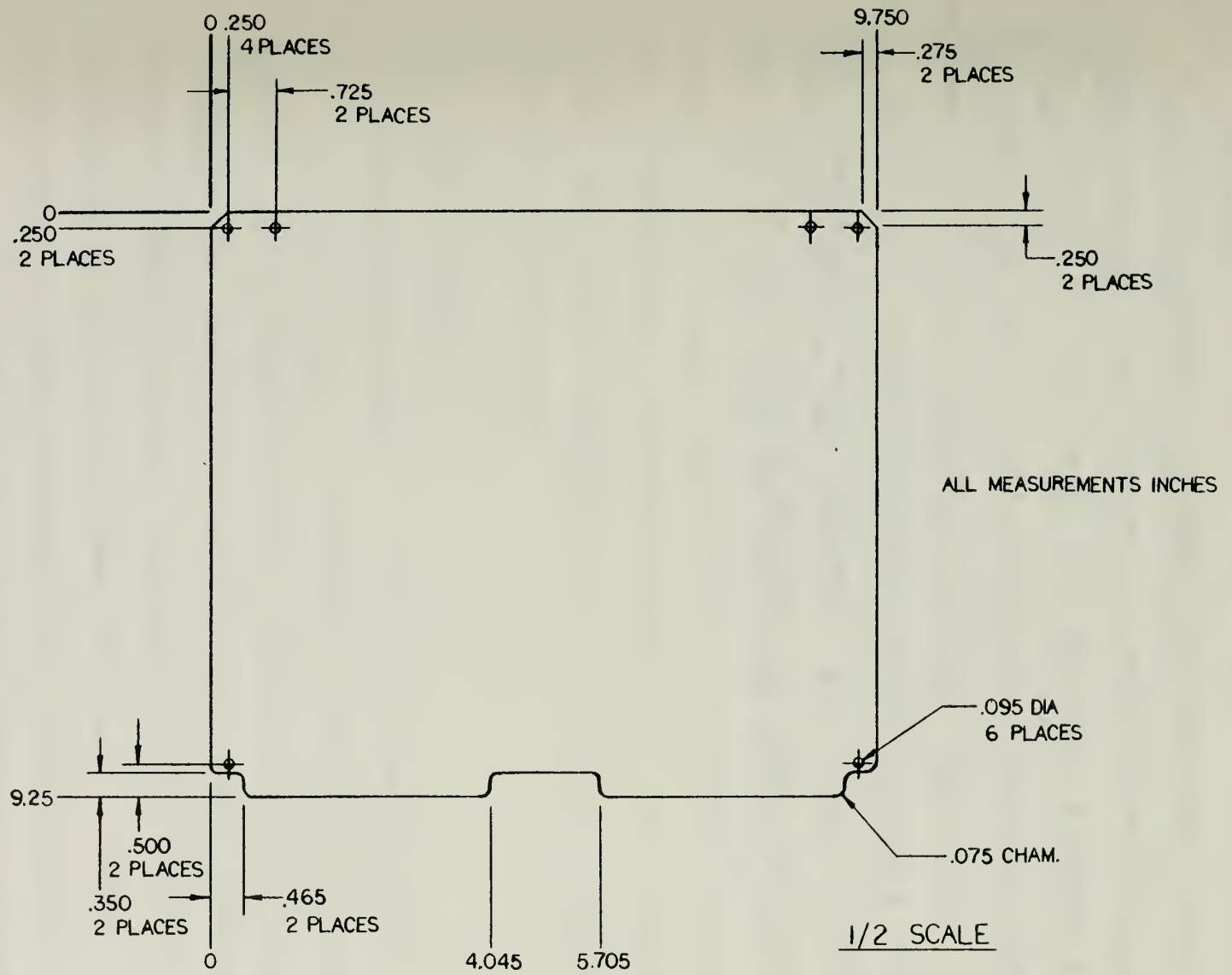


Figure 3.3

Control Bus Interface
Printed Circuit Board
Size Template

KF 5/24/78

and the logic elements are placed in rows. An attempt to keep chips requiring large numbers of connections close to the board edges resulted in a neater layout, however, some chip placements were made with regard only to proximity of the edge connector. Horizontal runs of foil were restricted to the top or component side of the board as muct as possible. Vertical runs were made on the bottom side. This scheme allowed all connections to be made on the board itself, and only one wire jumper was required on the entire board.

IV. ASSEMBLY

A. COMPONENTS

Table I lists all components used on the Control Bus Interface Board. The parts placement is given in Figure 4.1. As mentioned previously, construction time runs approximately two hours per board if the IC sockets are pre-soldered and the board is of the plated-through type. One-fourth watt resistors are sufficient for all cases, and types of capacitors used does not seem critical. Disc ceramic capacitors were used in most cases and no problems were encountered even in the critical timing applications. The same is true for all PC boards used in the Control Bus. The only exceptions to the Disc ceramic capacitor occurs at C1 and C2 where electrolytics are required.

B. LESSONS LEARNED

Problems encountered in assembly were misalignment of the IC's in their sockets or placement of the IC's in the wrong sockets. It is suggested that a technician other than the one performing assembly be assigned to check IC placement. Further, a check on correct placement of all components is recommended before applying power for tests. Assembly of a large number of boards becomes quite tedious and generally more mistakes are made on the later constructed boards due to complacency. For that reason, several technicians working on a small number of boards each may be more productive than assigning one to do them all.

TABLE I

CONTROL BUS INTERFACE BOARD COMPONENTS

C1,2	1Ø mfd., 12 VDC Electrolytic Capacitors
C3,4,5,6,7,8,9,1Ø	.Ø5 mfd. Disc Ceramic Capacitors
C11	.ØØ1 mfd. Disc Ceramic Capacitor
C12	47 pf. Disc Ceramic Capacitor
C13	33Ø pf. Disc Ceramic Capacitor
IC1,2,13,15,27	74ØØ TTL Integrated Circuit
IC3,4,16,17,18,24	74Ø4 TTL Integrated Circuit
IC5	7411 TTL Integrated Circuit
IC6,19	741Ø TTL Integrated Circuit
IC,7,8,9,1Ø	74153 TTL Integrated Circuit
IC11,12,14,22	7438 TTL Integrated Circuit
IC2Ø	742Ø TTL Integrated Circuit
IC21,28,25	7474 TTL Integrated Circuit
IC23	74123 TTL Integrated Circuit
R1,2,3,4,5,6,7,8	1ØØØ ohm, 1/4 watt Resistors
R9	1ØØ ohm, 1/4 watt Resistors
R1Ø,11	68ØØ ohm, 1/4 watt Resistors
SA1,2	GRAYHILL 76CØ4 SPDT Switch Assembly

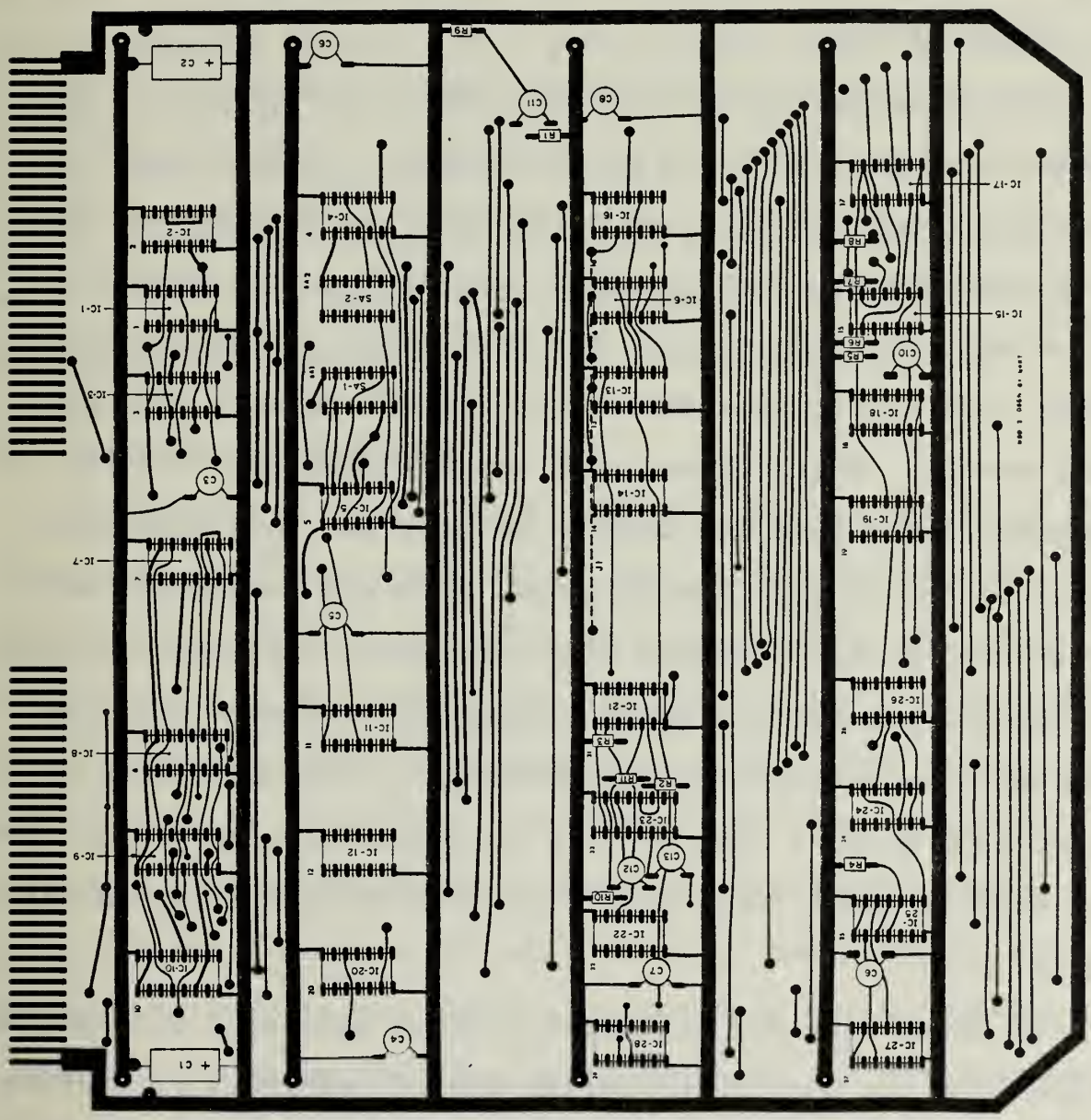


Figure 4.1

Parts Placement

V. TESTING

A. STATIC TESTS

The ability to statically test each PC assembly in the Control Bus has proven to be invaluable. In the beginning, computer run diagnostics were required for testing and the operating system had to be shut down during this period. Troubleshooting the Control Bus then became competitive with other work requiring computer use and delays were suffered as a result. Static tests were conducted by removing the computer cable from the CAMBION Chassis and this completely isolated the Control Bus hardware. The A29 Interface Test panel and the A36 Computer Simulator Panel were then connected to the bus and testing began. Appendix A gives a detailed step-by-step procedure for conducting a thorough static test. After each step, a list of IC's is included which could cause the problem should that step fail to produce the desired results.

To date, very few hardware problems have been encountered which were not duplicated during static testing. It must be noted, however, that the logic elements on the bus are not exercised at computer speeds during these tests. Therefore, there may be failures which will only appear during computer run diagnostics.

Later developments in the evolution of the SATCOM Signal Analyzer dictated a need for a method by which static testing

could be performed without removing the Control Bus from the computer. Therefore, the last two slots on the bottom rack of the CAMBION Chassis [2] were isolated from the bus via backplane wiring and static testing may now be conducted using these slots in conjunction with the A29 Interface Test Panel and the A36 Computer Simulator Panel. This scheme works quite effectively and allows testing to be performed completely independent of overall system requirements.

B. COMPUTER DIAGNOSTICS

Diagnostic software for the Control Bus hardware has been developed [8] and works well. The primary advantage of having this software available is being able to run tests on bus logic at the computer's operating speed. Many conditions such as crosstalk between data lines, line reflections which produced "glitches", and others have been isolated with the diagnostic software which did not appear during static tests. Another valuable asset of the computer run diagnostic test is the ability to put data out on the bus repetitively while checking waveforms with an oscilloscope. This "looping" of the data simulates what happens on the bus in real-time use.

The computer run diagnostic is easy to load [8] and results have been gratifying. It is apparent that neither of these troubleshooting aids alone would be sufficient, but used together they are extremely effective.

VI. IMPLEMENTATION

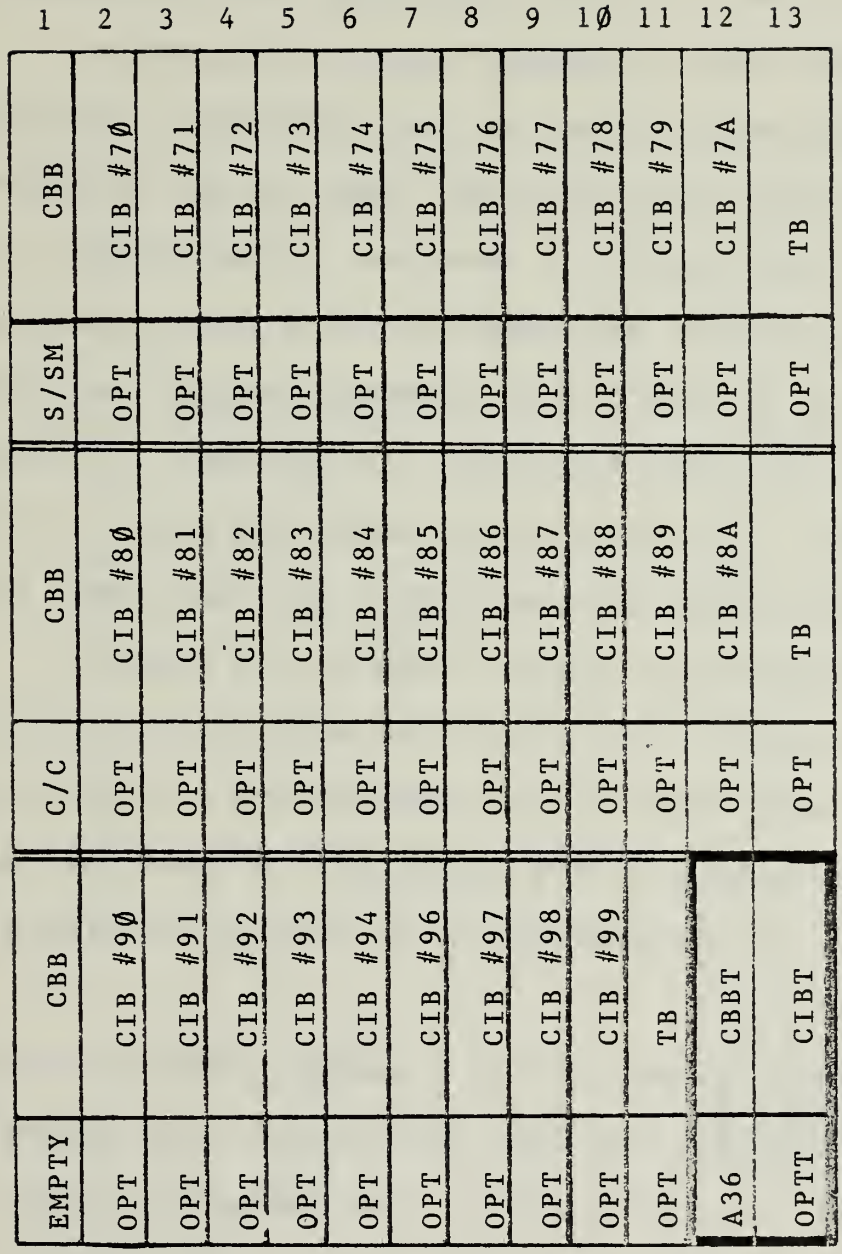
A. CAMBION CHASSIS AND WIRING

Pin-to-pin connections on the backplane of the CAMBION 714 and 715 chassis [2] remain unchanged except for three specific slots.

Figure 6.1 shows the configuration of the CAMBION chassis as presently installed in the rack. The first slot to be altered was the number one slot in the topmost CAMBION 715 chassis. This slot now provides connections to the special purpose SCLRO/SATNO Monitor Board. This board provides a means of clearing any interrupts which may be pending service from the computer.

The requirement for this function resulted from problems encountered when powering the CAMBION chassis up or down. Whenever the power was interrupted at the CAMBION chassis, computer "crashes" occurred. If any device on the Control Bus generates an interrupt signal the computer will eventually return to the bus and attempt to service that interrupt. If power is secured while the computer is attempting to communicate with a device or service an interrupt, a system "crash" will occur. System crashes will occur on power up as well since unsolicited interrupts may be generated due to the randomness of the flip-flop states. When one of these unsolicited interrupts occurs, the computer will attempt to determine the address of the device requesting attention.

Slot Number



1	2	3	4	5	6	7	8	9	10	11	12	13
EMPTY	CBB	C/C	CBB	S/SM	CBB							
OPT	CIB #90	OPT	CIB #80	OPT	CIB #70							
OPT	CIB #91	OPT	CIB #81	OPT	CIB #71							
OPT	CIB #92	OPT	CIB #82	OPT	CIB #72							
OPT	CIB #93	OPT	CIB #83	OPT	CIB #73							
OPT	CIB #94	OPT	CIB #84	OPT	CIB #74							
OPT	CIB #96	OPT	CIB #85	OPT	CIB #75							
OPT	CIB #97	OPT	CIB #86	OPT	CIB #76							
OPT	CIB #98	OPT	CIB #87	OPT	CIB #77							
OPT	CIB #99	OPT	CIB #88	OPT	CIB #78							
OPT	TB	OPT	CIB #89	OPT	CIB #79							
A36	CBBT	OPT	CIB #8A	OPT	CIB #7A							
OPTT	CIBT	OPT	TB	OPT	TB							

CBB - Control Bus Buffer Board (T) Test Board
CIB - Control Bus Interface Board (T) Test Board
S/SM - SCLRO/SATNO Monitor Board
C/C - Computer Cable Card
OPT - Option Board
A36 - Calbe Card To Computer Simulator Panel
TB - Terminator Board

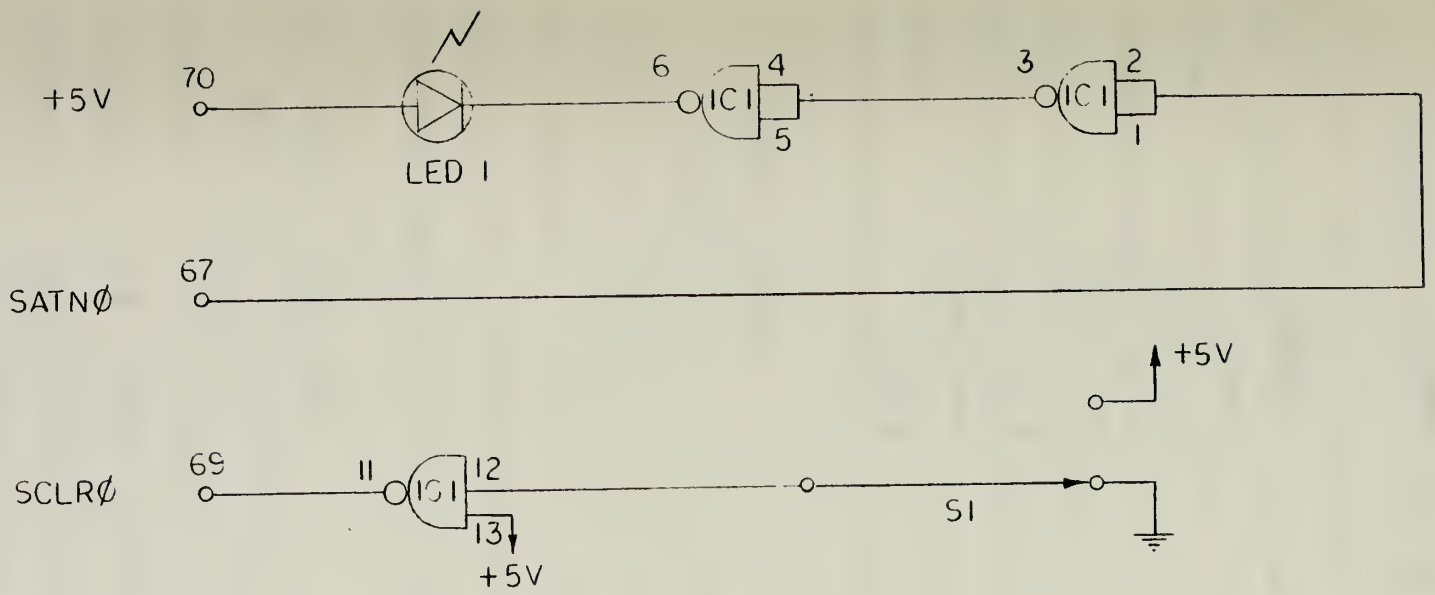
Figure 6.1

Rack Configuration

Since no device on the bus generated the interrupt, the computer receives a "garbage" reply and crashes.

The simplest solution to these problems involved installation of a light emitting diode (LED) on the interrupt line (SATNO), a push button to generate a clear (SCLRO) signal, and a bus switch on the computer cable card. Before bringing power up or down at the CAMBION chassis, the SCLRO button is held in while the bus switch is toggled. If interrupts were pending (indicated by the SATNO LED being ON) they are immediately cleared by the SCLRO signal and power up or down can be accomplished without crashing the computer. Figure 6.2 is a schematic diagram of the SCLRO/SATNO Monitor Board. Table II shows wire-wrap pin connections for the SCLRO/SATNO Monitor Board made on the backplane. A detailed procedure on powering the Control Bus up or down is contained in Appendix B.

The other changes to the original CAMBION chassis wiring consists of wiring the last two slots in the bottom 714 and 715 chassis for static tests. The backplane wiring for these slots is identical to the rest of the chassis except that they are completely isolated from the Control Bus. As a result, there now exists a static test slot for a Control Bus Buffer Board /‾5‾/, a Control Bus Interface Board, and an Option Board of choice. The A29 Interface Panel plugs into the Option Board connector directly, and the A36 Computer Simulator Panel plugs into the slot immediately below



DRAWING NO. 535A15-A29-75	NAVAL POSTGRADUATE SCHOOL
DRAWN	INTERRUPT MONITOR/CLEAR
APPROVED	

Figure 6.2

SCLRO/SATNO Monitor Board Schematic

TABLE II

BACKPLANE CONNECTIONS
FOR SCLRO/SATNO MONITOR BOARD

PIN NO.	NAME
35	Ground
36	Not Used
|	
66	Not Used
67	SATNO
68	Not Used
69	SCLRO
7Ø	+ 5v

the Control Bus Buffer Board.

B. OPTION BOARDS

Presently, there exist three different Option Boards [5] and they are designated A, B, or C as shown in Table IV. These boards are designed to interface with specific types of equipment, however, the pin-out of each board is identical since the backplane wiring at each Option Board slot in the CAMBION chassis is the same. Each Option Board contains an end connector to which the cabling between the board and the device is attached. A detailed description of each Option Board is contained in [5].

C. BUFFER BOARDS

A Control Bus Buffer Board is used in each CAMBION 714 chassis to isolate all devices operated by that chassis from the remainder of the bus. Additional drive for TTL logic gates is also provided using 7438 driver IC's. This board occupies the first slot in each CAMBION 714 chassis.

D. STATIC TEST SLOTS

The static test slots are the last two slots in the bottom 714 and 715 chassis. Residing in these slots is usually a set of known good boards. Therefore, there should always be a spare Control Bus Buffer Board, Control Bus Interface Board, and Option Board A, if another needs replacing. These boards are normally used for trouble-shooting only and

should not be used ordinarily. However, if one should be used, the defective board should be repaired as quickly as possible in order to return the test board to its proper position. This will prevent accumulation of defective boards in the static test slots which will impair the ability to quickly perform tests.

E. BACKPLANE

All backplane wiring [2] is wire-wrapped and has proven to be virtually maintenance free. A plexiglass cover has been fastened across the back of the rack in order to protect the pins and wiring. Most wire-wrap pins are relatively long and bend easily. In addition, wire used on the backplane is small gauge and sometimes easily snagged. The backplane cover has prevented inadvertent shorts or accidental loosening of mechanically fragile wire-wrap connections.

F. DEVICE ADDRESSES

Device addresses on the Control Bus were chosen carefully so as not to duplicate other addresses currently in use on the 7/32 multiplexer bus. These addresses are labelled above each slot and selected by small switch assemblies located on the Control Bus Interface Board [2].

Several hardware related problems have been traced to having two or more Control Bus Interface Boards resident on the bus with identical addresses. It is imperative that all Control Bus Interface Boards installed have unique addresses,

otherwise, results of control signals sent to the controlled device will be totally unpredictable.

Table III shows device addresses by slot number as currently programmed. Gaps in the sequence of addresses are due to prior assignment to other devices in the system.

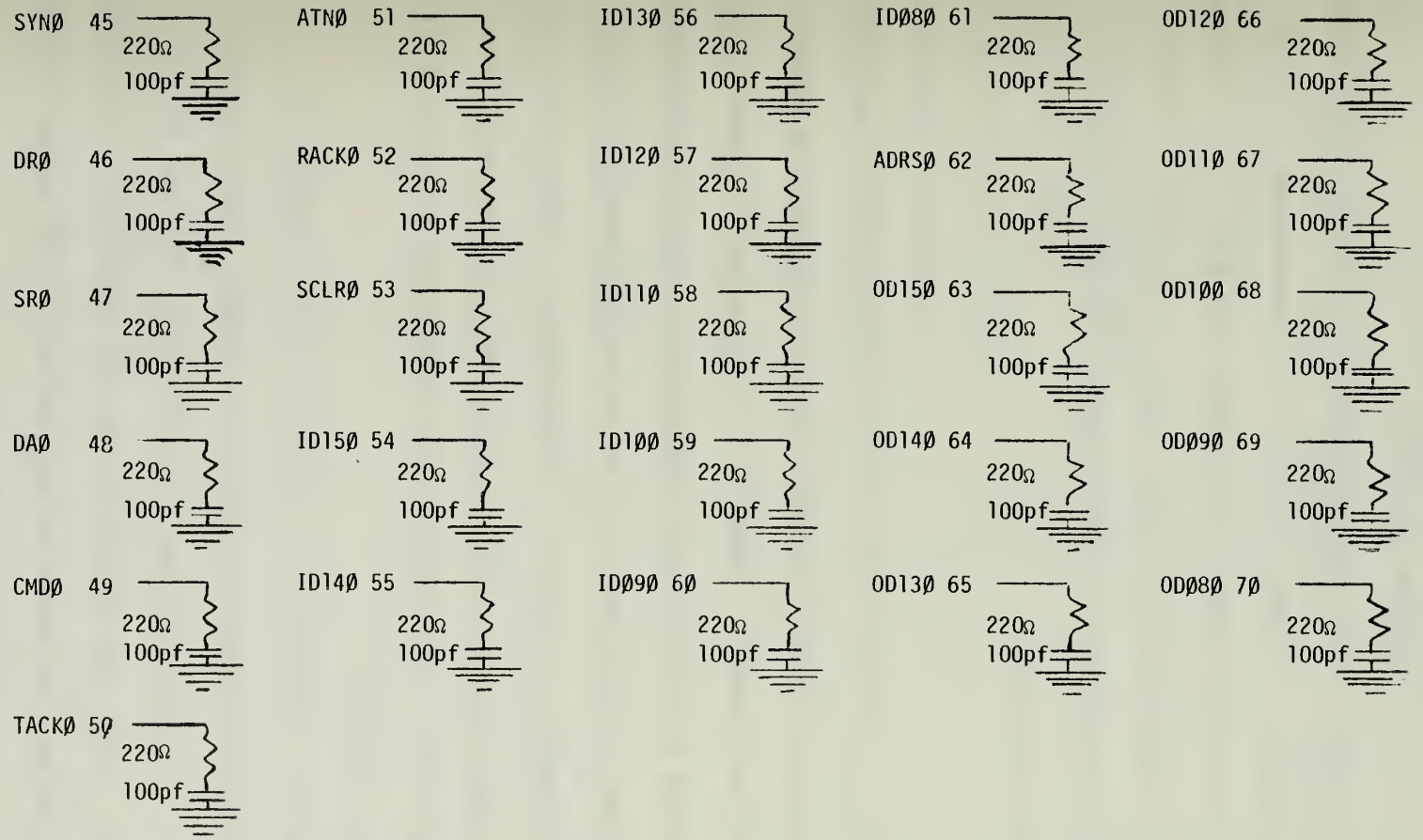
G. BUS TERMINATION

In accordance with [9], each command, control, and data line is terminated to eliminate reflections and/or "glitches" on the bus. Figure 6.3 is the schematic for the Bus Termination Board which is installed in the last active slot in each CAMBION 714 Chassis.

TABLE III

DEVICE ADDRESSES

SLOT NO.	ADDRESS	DEVICE
TOP CHASSIS		
# 2	70	NONE
# 3	71	NONE
# 4	72	NONE
# 5	73	NONE
# 6	74	NONE
# 7	75	NONE
# 8	76	NONE
# 9	77	NONE
#10	78	NONE
#11	79	NONE
#12	7A	NONE
MIDDLE CHASSIS		
# 2	80	C1 Control Panel
# 3	81	C2 Control Panel
# 4	82	C4 Control Panel
# 5	83	A6 Primary Reciever
# 6	84	A10/12 Probe Receivers
# 7	85	A25 Spectrum Receiver
# 8	86	A24 Rockland Filter
# 9	87	NONE
#10	88	NONE
#11	89	NONE
#12	8A	NONE
BOTTOM CHASSIS		
# 2	90	A18 Fluke Synthesizer
# 3	91	A19 Fluke Synthesizer
# 4	92	A8 Fluke Synthesizer
# 5	93	A14 Fluke Synthesizer
# 6	94	A21 Fluke Synthesizer
# 7	96	NONE
# 8	97	NONE
# 9	98	NONE
#10	99	NONE



DRAWING NO. 535A15-A29-80	NAVAL POSTGRADUATE SCHOOL
DRAWN Mell	
APPROVED	BUS TERMINATION BOARD SCHEMATIC

Figure 6.3

Bus Termination Board Schematic

VII. OPERATION

A. PERIPHERALS UNDER PROGRAM CONTROL

To date, thirteen external devices have been integrated under program control. These devices are accessed through the Control Bus Interface and are listed in Table IV, along with the type of Option Board each device requires. Few hardware problems have been encountered and the interface has proven very effective.

B. FAILURES

The few failures which have occurred have been due primarily to IC failure either on the Control Bus Interface Board or the Option Board. However, the overall design has proven to be sound and much less expensive than alternative solutions considered earlier. The primary cause of chip failure is due simply to use of inexpensive, common TTL IC's. Other designs using special IC's may have proven more reliable but would have been much more costly and sources of supply much less common.

Foil connector "fingers" or contacts on certain PC boards have actually been the source of more hardware failures than IC's. Of six option boards which failed upon initial testing, only two were due to IC failure. The solution to this problem has been elimination of PC board stock with pre-etched, gold-plated contacts.

TABLE IV

DEVICES UNDER PROGRAM CONTROL

DEVICE	ADDRESS	OPTION BOARD
C1 Control Panel	80	A
C2 Control Panel	81	A
A14 Fluke Synthesizer	93	C
C4 Control Panel	82	A
A25 Spectrum Receiver	85	A
A6 Primary Receiver	83	A
A18 Fluke Synthesizer	90	C
A8 Fluke Synthesizer	92	C
A10/12 Probe Receivers	84	A
A21 Fluke Synthesizer	94	C
A24 Rockland Filter	86	B

Overall, hardware reliability of the Control Bus Interface is exceedingly good. With the design of built-in trouble-shooting aids (static tests, computer diagnositcs, etc.), any faults which do occur are quickly and easily isolated without need to shut-down the system.

VIII. CONCLUSION

A viable, effective and relatively inexpensive solution to bus expansion of the INTERDATA 7/32 multiplexer bus has been demonstrated. This report is the last of a series [2,5] concerning design, fabrication and testing of the SATCOM Signal Analyzer Control Bus Interface. It is evident that in-house adaptation of the original INTERDATA Universal Logic Interface design has proven successful. Future efforts will involve exploring ways to utilize the program control capability for various peripheral devices.

APPENDIX A

PROCEDURE FOR CONTROL INTERFACE BOARD STATIC TESTS

1. Ensure power switch is ON and observe power lights on the Computer Simulator Panel (A36) and the Interface Test Panel (A29) are ON.
2. Install the Board under test into proper test slot. Be sure that the remaining boards in the test slots are good.
3. Cycle A36 SCLRO switch and A29 CLR switch.
4. Set switches Ø, 3, 5 and 7 on A36 DATA OUT switches. Reset all other DATA OUT switches.
5. Set A36 ADRSO switch.
6. Observe A36 SYNO light OFF.
7. Reset A36 ADRSO switch.
8. Set Interface Board address on A36 DATA OUT switches.
9. Set A36 ADRSO switch.
10. Observe A36 SYNO Light ON. (IC 1,2,3,4,5,6,20,21,22,23).
11. Reset A36 ADRSO switch.
12. Observe A36 SYNO light OFF (IC 20,21,22,23).
13. Set Switch #1 on A36 DATA OUT switches; reset all other A36 DATA OUT switches.
14. Set A36 CMDO switch.
15. Observe A36 SYNO Light ON (Same as step 10).
16. Observe A29 CM Light is ON (IC 15,16,17).
17. Cycle A29 CLR switch; reset A36 CMDO switch.
18. Observe A29 CM Light and A36 SYNO Light are OFF.

19. Cycle A29 INT switch.

20. Observe A36 INT Light is ON. (IC 14,20,21,23,24,25,26).

21. Set A36 ACKO switch.

22. Observe A36 SYNO and INT Light are ON, and Interface Board address is displayed on A36 DATA IN lights. (Same as steps 10,20 plus IC 7,8,9,10,11,12).

23. Observe A29 RA light is ON.

24. Cycle A29 CLR switch.

25. Observe A29 RA light is OFF.

26. Reset A36 ACKO switch.

27. Observe A36 SYNO, INT, and DATA IN lights are OFF.

28. Set Switch #Ø on A36 DATA OUT switches; reset all other DATA OUT switches.

29. Set A36 CMDO switch.

30. Observe A29 CM Light and A36 SYNO Light is ON, (Same as step 10,16).

31. Cycle A29 CLR switch.

32. Observe A29 CM Light is OFF.

33. Reset A36 CMDO switch.

34. Observe A36 SYNO light is OFF.

35. Cycle A29 INT switch.

36. Observe A36 INT light is OFF. (IC 3,20,25,27).

37. Set Switch #1 on A36 DATA OUT switches; reset all other DATA OUT switches.

38. Set A36 CMDO switch.

39. Observe A36 SYNO and INT light are ON. (Same as steps 10,20,36).

40. Reset A36 CMDO switch.

41. Observe A36 SYNO light is OFF and INT light remains ON. (Same as step 20).

42. Observe A29 CM light is ON (Same as step 16).

43. Cycle A29 CLR switch.

44. Observe A29 CM light is OFF.

45. Repeat steps 21 through 27.

46. Set switches #Ø and #1 on A36 DATA OUT switches; reset all other DATA OUT switches.

47. Set A36 CMDO switch.

48. Observe A36 SYNO light and A29 CM light are ON. (Same as steps 10,16).

49. Reset A36 CMDO switch.

50. Observe A36 SYNO light OFF.

51. Cycle A29 CLR switch.

52. Observe A29 CM light OFF.

53. Cycle A29 INT switch.

54. Observe A36 INT light OFF. (Same as step 20).

55. Set Switch #1 on A36 DATA OUT switches; reset all other DATA OUT switches.

56. Set A36 CMDO switch.

57. Observe A36 SYNO light and A29 CM light are ON (Same as steps 10,16).

58. Observe A36 INT light OFF (Same as step 20).

59. Reset A36 CMDO switch.

60. Cycle A29 CLR switch.

61. Observe A36 SYNO light and A29 CM light are OFF.

62. Set ALL A36 DATA OUT switches.

63. Set A36 DAO switch.

64. Observe A36 SYNO light and A29 DA light are ON. (IC 13, 16,17,20,21,22,23).

65. Observe ALL A29 DATA OUT lights are ON. (Same as step 22).

66. Reset ALL A36 DATA OUT switches.

67. Observe ALL A29 DATA OUT lights are OFF.

68. Reset A36 DAO switch.

69. Cycle A29 CLR switch.

70. Observe A36 SYNO light and A29 DA light are OFF.

71. Set ALL A29 DATA IN switches.

72. Set A36 DRO switch.

73. Observe A36 SYNO light and ALL A36 DATA IN lights are ON (Same as step 22).

74. Observe A29 DR light ON (IC 15,17,18).

75. Reset ALL A29 DATA IN switches.

76. Observe ALL A36 DATA IN lights are OFF.

77. Reset A36 DRO switch.

78. Cycle A29 CLR switch.

79. Observe A36 SYNO light and A29 DR light are OFF.

80. Set Switches #2 through #7 on A29 STATUS IN switches.

81. Set A36 SRO switch.

82. Observe A36 SYNO light ON (Same as step 10).

83. Observe lights #2 through #7 on A36 DATA IN lights are ON (Same as step 22).

84. Observe A29 SR light ON (Same as step 74).

85. Reset ALL A29 STATUS IN switches.

86. Observe ALL A36 DATA IN lights are OFF.

87. Reset A36 SRO switch.

88. Cycle A29 CLR switch.

89. Observe A36 SYNO light and A29 SR light are OFF.

90. Set Switches #4 through #7 on A36 DATA OUT switches; reset ALL other DATA OUT switches.

91. Set A36 CMDO switch.

92. Observe A36 SYNO light ON (Same as step 10).

93. Observe A29 CM light ON (Same as step 16).

94. Observe ALL A29 COMMAND lights are ON (Same as step 22).

95. Reset ALL A6 DATA OUT switches.

96. Observe ALL A29 COMMAND lights are OFF.

97. Reset A36 CMDO switch.

98. Cycle A29 CLR switch.

99. Observe A36 SYNO light and A29 CM light are OFF.

100. THIS COMPLETES THE TEST.

APPENDIX B

TO POWER DOWN

1. Hold SCLRO Button IN
2. While holding button IN, turn bus switch on cable card OFF
3. Now, turn power switch OFF.

TO POWER UP

1. Turn Power ON
2. Hold SCLRO Button IN and turn bus switch ON

LIST OF REFERENCES

1. Charles B. Williams and John E. Ohlson, Receiver Design for the Naval Postgraduate School SATCOM Signal Analyzer, Technical Report NPS62-78-002, Naval Postgraduate School, Monterey, January 1978.

2. Gary W. Bohannan and John E. Ohlson, Digital Control and Processing for a Satellite Communications Monitoring System, Technical Report NPS62-78-001, Naval Postgraduate School, Monterey, January 1978.

3. James D. Zuber, Jr. and John E. Ohlson, Hardware Development for a Satellite Signal Analyzer, Technical Report NPS62-78-004PR, Naval Postgraduate School, Monterey, March 1978. (CONFIDENTIAL)

4. Marvin J. Langston and John E. Ohlson, Data Acquisition Unit for the SATCOM Signal Analyzer, Technical Report in progress, Naval Postgraduate School, Monterey, June 1978.

5. Bobbie George Edgington and John E. Ohlson, System Development for Satellite Oscillator Stability Measurements, Technical Report in progress, Naval Postgraduate School, Monterey, June 1978.

6. William A. Rhoades and John E. Ohlson, Integration of the Primary Receiver into the NAVPGSCOL SATCOM Signal Analyzer, Technical Report in progress, Naval Postgraduate School, Monterey, June 1978.

7. Richard R. Mead and John E. Ohlson, Digital Control and Interfacing for a High Speed Satellite Communications Signal Processor, Technical Report in progress, Naval Postgraduate School, Monterey, September 1978.

8. Todd T. W. Bruner and John E. Ohlson, Software Development for a Satellite Signal Analyzer, Technical Report in progress, Naval Postgraduate School, Monterey, September 1978.

9. INTERDATA, Inc., I/O Interface Design Standards, Publication Number 43-009, October 1975.

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